D 40973 (Pages : 2) Name.....

Reg. No.....

SIXTH SEMESTER B.Sc. DEGREE (SUPPLEMENTARY) EXAMINATION MARCH 2018

(CCSS)

CS 6B 15—COMPUTER ORGANIZATION AND ARCHITECTURE

(2012 Admissions)

Time : Three Hours Maximum : 30 Weightag

I. Answer all *twelve* questions :

1 ——— is a group of bits that instructs the computer to perform a specific operation.

2 MIMD stands for ———.

3 Execution of two or more programs by a single CPU is known as ———.

4 Zero address instruction format is used for :

(a) RISC architecture. (b) CISC architecture.

(c) Von Neuman architecture. (d) Stack organized architecture.

5 A control unit whose binary control variables are stored in memory is called ———.

6 The addressing mode in which the operands are specified implicitly in the instruction is call ———.

7 BCD is ———.

8 Write Through technique is used in which memory for updating the data :

(a) Virtual memory. (b) Main memory.

(c) Cache memory. (d) Auxiliary Memory.

9 ——— algorithm gives a procedure for multiplying binary integer in signed -2's compleme representation.

10 Input or output devices attached to the computer are also called ———.

11 ——— is a program control instruction.

(a) IN. (b) SETC.

(c) SKIP. (d) None of these.

Turn ov

12 In GRO, when the binary code for selector A is 000 then the multiplexer A selects input from _____.

(12 × ¼ = 3 weightage)

II. Answer all *nine* questions :

13 What is the difference between direct and indirect address instruction ?

14 What is computer architecture ?

15 Define ASCII code.

16 What is instruction pipelining ?

17 Define virtual memory ? Why is it used ?

18 What is microprogrammed control ?

19 Define fetch cycle and instruction cycle.

20 What is cache memory ?

21 How an interrupt is recognized ? Explain the interrupt cycle.

(9 × 1 = 9 weightage)

III. Answer any *five* questions :

22 Explain any four memory reference instructions

23 Explain the implementation of stack in CPU.

24 What are peripherals ? Explain different types of peripherals.

25 What is associative memory ? Explain the block diagram of associative memory ?

26 Explain the block diagram of a typical DMA controller.

27 Explain the memory hierarchy in a computer system.

28 Explain dynamic pipeline.

(5 × 2 = 10 weightage)

IV. Answer any *two* questions :

29 With the help of block diagrams explain RAM and ROM organization ?

30 Explain the bus organization for seven CPU registers with the help of a neat diagram.

31 What is meant by an arithmetic pipeline ? Give an example of a pipeline unit for floating point addition and subtraction ?

(2 × 4 = 8 weightage)