C 21647 (Pages : 2) Name.....

Reg. No.....

SIXTH SEMESTER B.Sc. DEGREE (SUPPLEMENTARY/IMPROVEMENT) EXAMINATION, MARCH 2016

(UG—CCSS)

Computer Science

CS 6B 15—COMPUTER ORGANIZATION AND ARCHITECTURE

(2012 Admission onwards)

Time : Three Hours Maximum : 30 Weightage

I. Answer all *twelve* questions :

1 A ———— is a set of instructions that specify the set of operations, operands and the sequence of processing.

2 Actual execution of instruction take place in a computer in ————.

3 The timing for all registers in the computer is controlled by ————.

4 The function of control unit in a digital computer is ————.

5 Memory unit accessed by content is called ————.

(a) Associative Memory. (b) Read Only Memory.

(c) Programmable memory. (d) Virtual Memory.

6 The register that keeps track of instructions in memory is :

(a) PC. (b) IR.

(c) AR. (d) AC.

7 The resister that holds the address for the stack is called a ————.

8 RPN is ————.

9 In a memory-mapped I/O system, which of the following will not be there ?

(a) LDA. (b) IN.

(c) ADD. (d) OUT.

10 The memory unit that communicate directly with CPU is called ————.

11 The pipeline that operates on a stream of instruction by overlapping the phases of instruction cycle is ————.

12 In DMA the data transfer is controlled by ————.

(12 × ¼ = 3 weightage)

Turn over

II. Answer all *nine* questions :—

13 Define instruction code and operation code.

14 Compare volatile and non-volatile memory. Give example for both.

15 Define a hardwired control organization ?

16 What is addressing mode ?

17 Define virtual memory ? Why is it used ?

18 What is parallel processing ?

19 Define implied mode ?

20 What is handshaking ?

21 Distinguish between address space and memory space ?

(9 × 1 = 9 weightage)

III. Answer any *five* questions :—

22 Explain the different phases of an instruction cycle ?

23 Explain the stored program organization.

24 Explain direct and indirect addressing modes.

25 Draw the flow chart for decimal division.

26 Explain the hardware implementation for sign magnitude addition and subtraction.

27 Explain the write through and write back process of cache memory.

28 Explain the difference between I/O processor and a data communication processor ?

(5 × 2 = 10 weightage)

IV. Answer any *two* questions :—

29 What are instruction formats ? Explain the various types.

30 Explain the various mapping procedures in the organization of cache memory.

31 Explain the basic parallel processing architecture and the structures SISD, SIMD, MISD and MIMD.

(2 × 4 = 8 weightage)